



Sheet 1

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO. 1687.1005	APPLICATION NO. 10/766,955
LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>		FIRST NAMED INVENTOR Hiroyuki YAMASHITA, et al.	FILING DATE January 30, 2004	
		GROUP ART UNIT		

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	TRANSLATION YES      NO	ABSTRACT
HR	AC	2000-259445	09/2000	Japan		x
HR	AD	2001-256072	09/2001	Japan		x
HR	AE	2002-175344	06/2002	Japan		x

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

TRANSLATION YES      NO
----------------------------

HR	AF	Sherwood, Timothy, et al., "Basic Block Distribution Analysis to Find Periodic Behavior and Simulation Points in Applications", International Conference on Parallel Architectures and Complication Techniques", September 2001.		
HR	AG	Knapp, D., et al., "Behavioral Synthesis Methodology for HDL-Based Specification and Validation", Proc. Design Automation Conf. June 1995.		
HR	AH	Ly, Tai, et al., "Scheduling Using Behavioral Templates", Proc. Design Automation Conf. June 1995.		
HR	AI	Gauthier, Lovic, et al., "Automatic Generation and Targeting of Application Specific Operating Systems and Embedded Systems Software", Proc. Design Automation and Test in Europe, March 2001.		
HR	AJ	Lyonnard, Damien, "Automatic Generation of Application-Specific Architectures for Heterogeneous Multiprocessor System-on-Chip", Proc. Design Automation Conf., June 2001.		

EXAMINER <i>Karen Rososhek</i>	DATE CONSIDERED <i>02/02/2006</i>
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

FORM PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO. 1687.1005	APPLICATION NO. 10/766,955
LIST OF REFERENCES CITED BY APPLICANT  (Use several sheets if necessary)				FIRST NAMED INVENTOR Hiroyuki YAMASHITA, et al.	
				FILING DATE January 30, 2004	GROUP ART UNIT

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	BA						
	BB						
	BC						
	BD						
	BE						
	BF						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES NO
	BG						
	BH						
	BI						
	BJ						
	BK						
	BL						

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

H.R	BM	Yoo, Sungjoo, et al., "Automatic Generation of Fast Timed Simulation Models for Operating Systems in SoC Design", Proc. Design Automation and Test in Europe, March 2002.
H.R	BN	Ikegami, Kurokawa, et al., "Analysis and Prospects for a C-based Behavioral System LSI Design Flow", IEICE 15th Workshop on Circuits and Systems in Karuzawa, April 22-23, 2002.
	BO	

EXAMINER <i>Glen Rossoshes</i>	DATE CONSIDERED <i>02/02/2006</i>
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	